FEATURES

- Compliant with IEEE802.3bs standard:
  400GAUI-8 electrical interface
- Compliant with IEEE 802.3bs standard:
- 400GBASE-DR4 optical interface
- Compliant with QSFP-DD MSA HW Rev 5.0
  Type 2 housing with MPO-12 connector
- Compliant with QSFP-DD CMIS Rev 4.0
- Supports 3dB channel insertion loss
- Maximum power consumption 12W
- Case operating temperature 0°C to 70°C
- Two wire serial Interface with digital diagnostic monitoring
- RoHS compliant
- Class 1 Laser

Module Characteristics

Table 1 – Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	T_S	-40	85	ºC	
Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensing)	RH	5	95	%	
Control Input Voltage	V_I	-0.3	V_{CC}+0.5	V	

Table 2 – Recommended Operating Conditions

Parameter	Symbo	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_{OPR}	0	-	70	ºC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	I_{CC_IP}	-	-	4800	mA	
Sustained peak current at hot plug	I_{CC_SP}	-	-	3960	mA	
Maximum Power Dissipation	P_D	-	-	12	W	
Maximum Power Dissipation, Low Power	P_{DLP}	-	-	1.5	W	
Signalling Rate per Lane	SRL	-	53.125	-	GBd	PAM4
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Power Supply Noise Tolerance (10Hz -	-	-	-	66	mV	
Rx Differential Data Output Load	-	-	100	-	Ohm	
Operating Distance	-	2	-	500	m	

Functional Characteristics (Optical)

The following tables list the performance specifications for the various functional blocks of the integrated optical transceiver module.

Table 3 – Transmitter Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Average Launch Power, each lane	AOP_L	-2.9	-	4	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each lane	T_{OMA}	-0.8	-	4.2	dBm	2
Launch Power in OMA_{outer} minus TDECQ, each lane	$T_{OMA-TDECQ}$	-2.2	-	-	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	3.4	dB	
Average Launch Power of OFF Transmitter, each lane	T_{OFF}	-	-	-15	dBm	
Extinction Ratio, each lane	ER	3.5	-	-	dB	
$RIN_{21.4}OMA$	RIN	-	-	-136	dB/Hz	
Optical Return Loss Tolerance	ORL	-	-	21.4	dB	
Transmitter Reflectance	T_R	-	-	-26	dB	3

Note 1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength

Note 2: Even if TDECQ < 1.4dB, OMAouter (min) must exceed this value

Note 3: Transmitter reflectance is defined looking into the transmitter

Table 4 – Receiver Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Damage Threshold, each lane	AOP_D	5	-	-	dBm	
Average Receive Power, each lane	AOP_R	-5.9	-	4	dBm	1
Receive Power (OMAouter), each lane	OMA_R	-	-	4.2	dBm	
Receiver Reflectance	RR	-	-	-26	dB	
Receiver Sensitivity (OMAouter), each lane	S_{OMA}	-	-	-4.4	dBm	2
Stressed Receiver Sensitivity (OMAouter), each lane	SRS	-	-	-1.9	dBm	3
Conditions of stressed receiver sensitivity test			-			
Stressed eye closure for PAM4 (SECQ)			3.4		dB	
OMAouter of each aggressor lane			4.2		dBm	

Note 1: Note 1: Average receive power, (min) is informative and not the principal indicator of signal strength

Note 2: Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB. Note 3: Measured with conformance test signal at TP3 for the BER = 2.4x10-4

Functional Characteristics (Electrical)

Table 5 – Electrical Specification High Speed Signal (compliant with IEEE 802.3bs 400GAUI-8)

Receiver (Module Output)						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Notes**
AC common-mode output Voltage (RMS)		-	-	17.5	mV	
Differential output Voltage		-	-	900	mV	
Near-end Eye height, differential		70	-	-	mV	
Far-end Eye height, differential		30	-	-	mV	
Far end pre-cursor ratio		-4.5	-	2.5	%	
Differential Termination Mismatch		-	-	10	%	
Transition Time (min, 20% to 80%)		9.5	-	-	ps	
DC common mode Voltage		-350	-	2850	mV	
Transmitter (Module Input)						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Notes**
Differential pk-pk input Voltage tolerance		900	-	-	mV	
Differential termination mismatch		-	-	10	%	
Single-ended voltage tolerance range		-0.4	-	3.3	V	
DC common mode Voltage		-350	-	2850	mV	

Table 6 – Electrical Specification Low Speed Signal (compliant with QSFP-DD HW Rev 5.0)

Parameter	**Symbol**	**Min.**	**Max.**	**Unit**	**Condition**
AC common-mode output Voltage (RMS)	V_{OL}	0	0.4	V	
Module Input SCL and SDA	V_{IL}	-0.3	V_{CC}*0.3	V	
	V_{IH}	V_{CC}*0.7	V_{CC}+0.5	V	
InitMode, ResetL and ModSelL	V_{IL}	-0.3	0.8	V	
	V_{IH}	2	V_{CC}+0.3	V	
IntL	V_{OL}	0	0.4	V	
	V_{OH}	V_{CC}-0.5	V_{CC}+0.3	V	

Pin Definitions

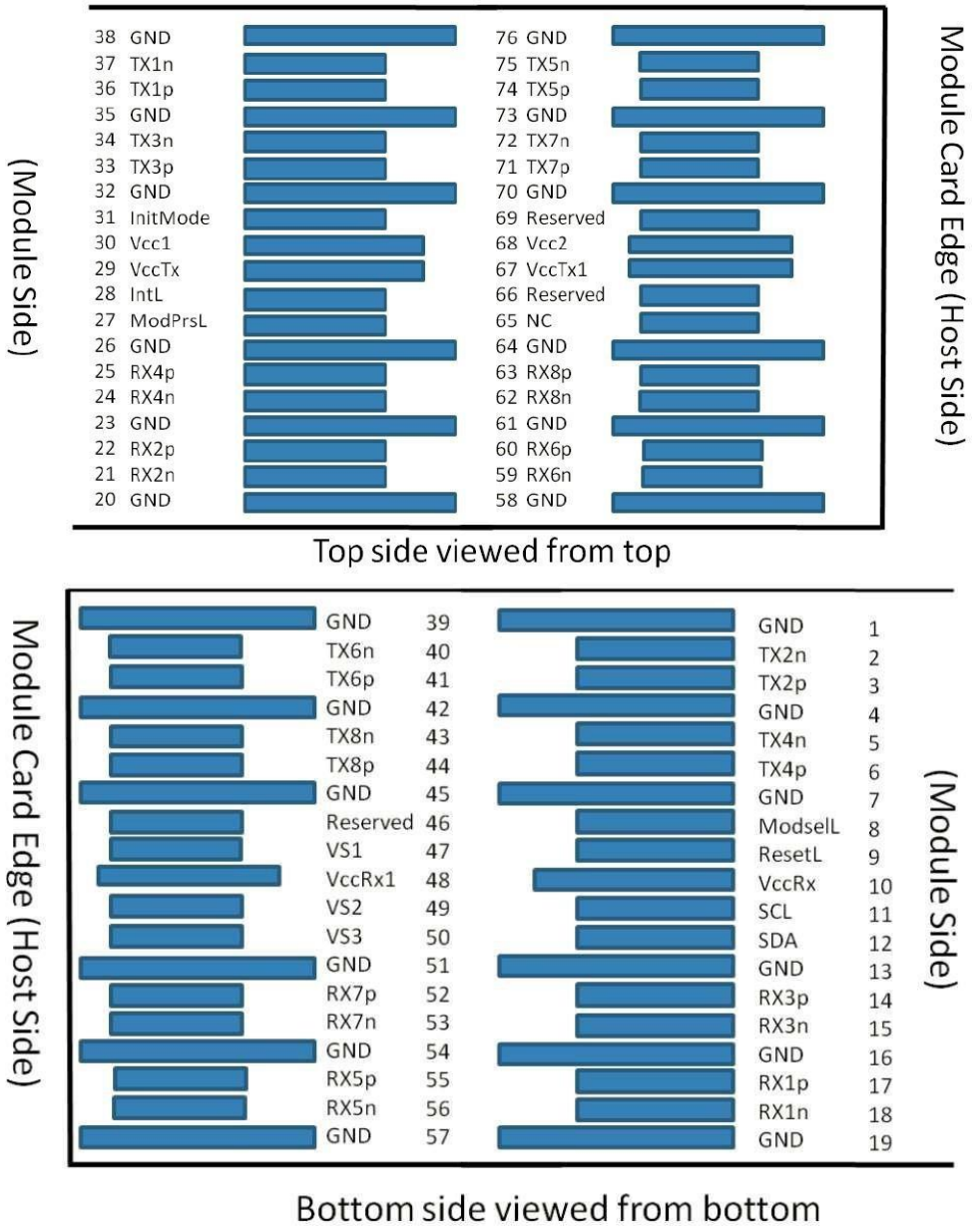


Figure 1 – Pin definitions of the module high speed inputs/outputs

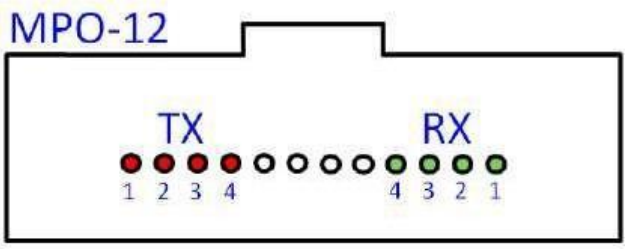


Figure 2 – Active fiber ports in MPO12 connector on module side

Table 7 – Module Pin Definitions

Pin #	Logic	Symbol	Definition	Pin #	Logic	Symbol	Definition
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46		Reserve	
9	LVTTL-I	ResetL	Module Reset	47		VS1	Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVCMOS	SCL	2-wire serial interface clock	49		VS2	Module Vendor Specific 2
12	LVCMOS	SDA	2-wire serial interface data	50		VS3	Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-	IntL	Interrupt	66		Reserv	
29		VccTx	+3.3V Power Supply Transmitter	67		VccTx1	3.3V Power Supply
30		Vcc1	+3.3V Power Supply	68		Vcc2	3.3V Power Supply
31	LVTTL-I	InitMode	Initialization mode	69		Reserv	
32		GND	Ground	70		GND	Ground
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73		GND	Ground
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76		GND	Ground

Recommended QSFP-DD Host Board Schematic

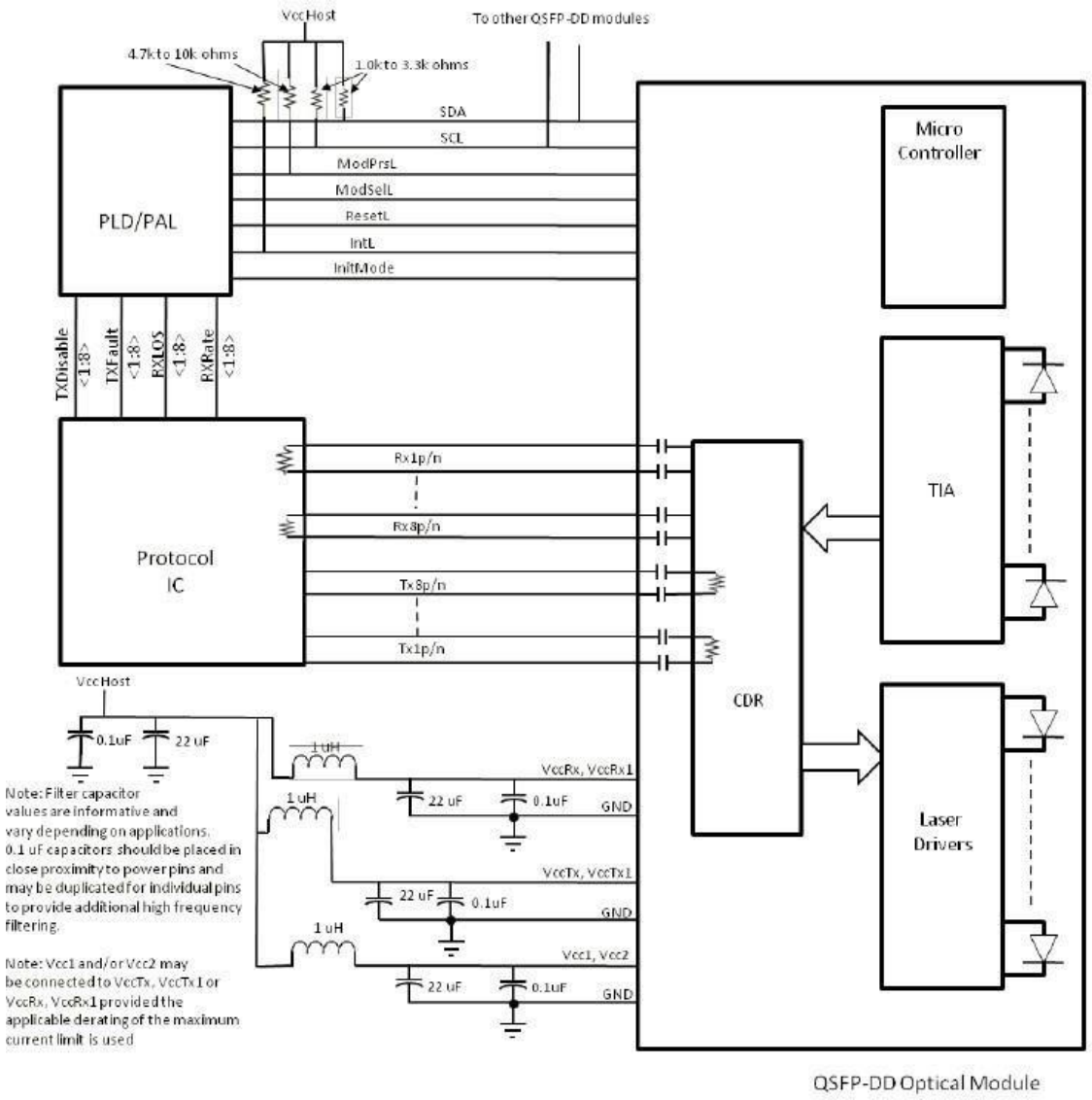


Figure 3 – Recommended QSFP-DD Host Board Schematic

Table 8 – Timing for Soft Control and Status Functions

Parameter	Symbol	Min.	Max.	Unit	Notes
MgmtInit Duration		-	2000	ms	
ResetL Assert Time	t_reset_init	10	-	µs	
IntL Assert Time	ton_IntL	-	200	ms	
IntL Deassert Time	toff_IntL	-	500	µs	
Rx LOS Assert Time	ton_los	-	100	ms	
Tx Fault Assert Time	ton_Txfault	-	200	ms	
Flag Assert Time	ton_flag	-	200	ms	
Mask Assert Time	ton_mask	-	100	ms	
Mask Deassert Time	toff_mask	-	100	ms	

Table 9 – I/O Timing for Squelch and Disable

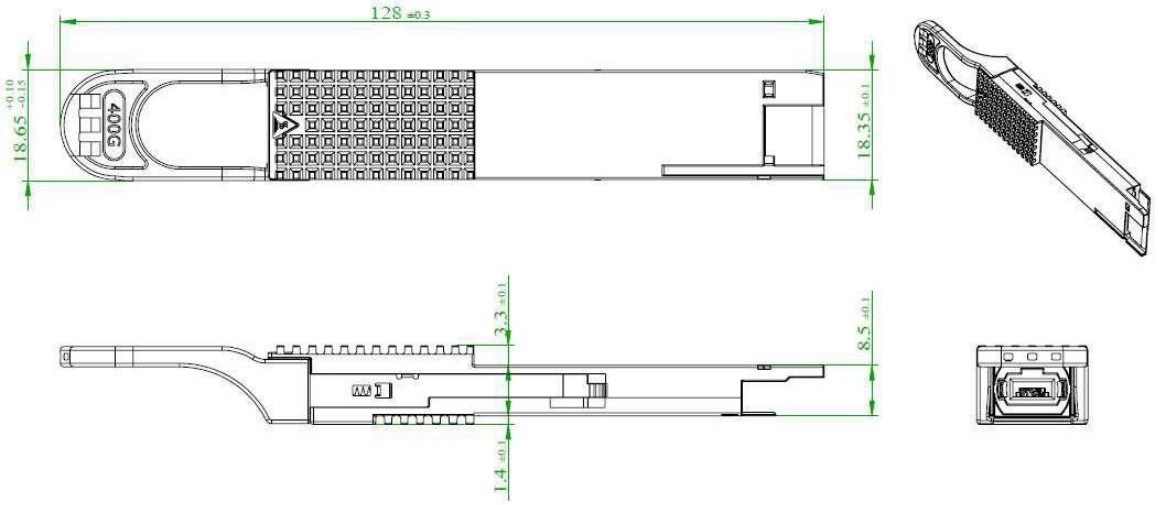
Parameter	Symbol	Min.	Max.	Unit	Notes
Rx Squelch Assert Time	ton_Rxsq	-	500	ms	Note
Rx Squelch Deassert Time	toff_Rxsq	-	15	s	Note
Tx Squelch Assert Time	ton_Txsq	-	400	ms	
Tx Squelch Deassert Time	toff_Txsq	-	5	s	Note
Tx Disable Assert Time	ton_Txdis	-	100	ms	
Tx Disable Deassert Time	toff_Txdis	-	400	ms	
Rx Output Disable Assert Time	ton_Rxdis	-	100	ms	
Rx Output Disable Deassert Time	toff_Rxdis	-	100	ms	
Squelch Disable Assert Time	ton_sqdis	-	N/A		Note, not support
Squelch Disable Deassert Time	toff_sqdis	-	N/A		Note, not support

Note: Timing not compliant with QSFP-DD-Hardware-rev5p0.

Table 10 – Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	0 to VCC	3%	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each	-2.9 to +4.0	±3	dB	Internal
Rx Receive Power (Each	-5.9 to +4.0	±3	dB	Internal

Mechanical Diagram



Ordering Information

Table 11 - Ordering Information

Part No.	Application	Data Rate	Laser Source	Fiber Type	Temperature
FWT-400G-05	400GBASE-DR4	400GB Ethernet	EML	Single Mode Fiber	0 ~ 70℃

WARNINGS

- Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.
- Laser Safety: Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.

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