Features:

- ✧ High-Density QSFP 38-PIN and 4×SFP 20-PIN Connector
- ✧ Hybrid cable conforms to the Small Form Factor SFF-8436 and SFF-8431
- ✧ Maximum aggregate data rate: 41.25Gbps (4 ×10.3125Gbit/s)
- ✧ Hybrid cable link length up to x(x=1,3,5,7m)
- ✧ Power Supply:+3.3V
- ✧ Low power consumption: 0.02 W (typ.)
- ✧ Temperature Range: 0~ 70°C

Applications:

- ✧ 10G/40Gigabit Ethernet
- ✧ InfiniBand SDR, DDR, QDR
- ✧ Switches, Routers, and HBAs
- ✧ Data Centers

Ordering information

PN	Description
FWTD-40G-4-01	QSFP+ To 4X SFP+ Passive Cables, 1m, 0ºC ~ +70ºC
FWTD-40G-4-03	QSFP+ To 4X SFP+ Passive Cables, 3m, 0ºC ~ +70ºC
FWTD-40G-4-05	QSFP+ To 4X SFP+ Passive Cables, 5m, 0ºC ~ +70ºC
FWTD-40G-4-07	QSFP+ To 4X SFP+ Passive Cables, 7m, 0ºC ~ +70ºC

Description:

The FWTD-40G-xxx QSFP+ to 4×SFP+ Passive cable assemblies are high performance, cost effective for SFP+ and QSFP+ equipment interconnects . The Hybrid cables are compliant with SFF-8436 and SFF-8431 specifications. It is offer a low power consumption, short reach interconnect applications. The cable each lane is capable of transmitting data at rates up to 10Gb/s, providing an aggregated rate of 40Gb/s.

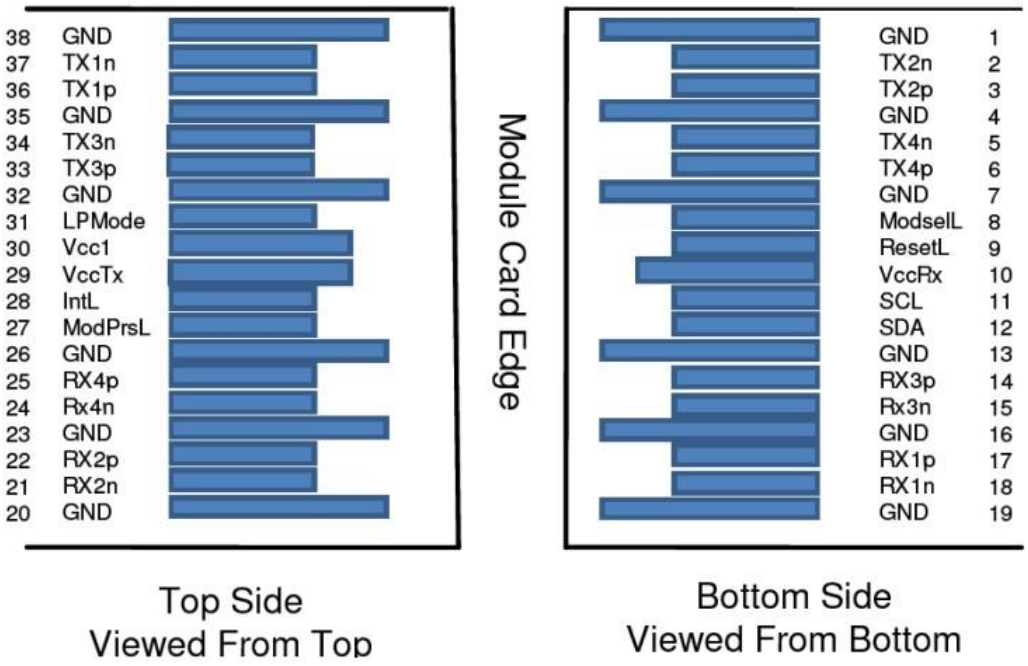
- **Absolute Maximum Ratings**

Parameter	Symbol	Min.	Typical	Max.	Unit
Storage Temperature	T_S	-40		+85	°C
Supply Voltage	$V_{CC}T$, R	-0.5		4	V
Relative Humidity	RH	0		85	%

Recommended Operating Environment:

Parameter	Symbol	Min.	Typical	Max.	Unit
Caseoperating Temperature	T_C	0		+70	°C
Supply Voltage	$V_{CCT, R}$	+3.13	3.3	+3.47	V
Power Dissipation	PD			0.02	W

QSFP+ Module Pad Layout



Top Side
Viewed From Top

Bottom Side
Viewed From Bottom

QSFP+ Pin Descriptions

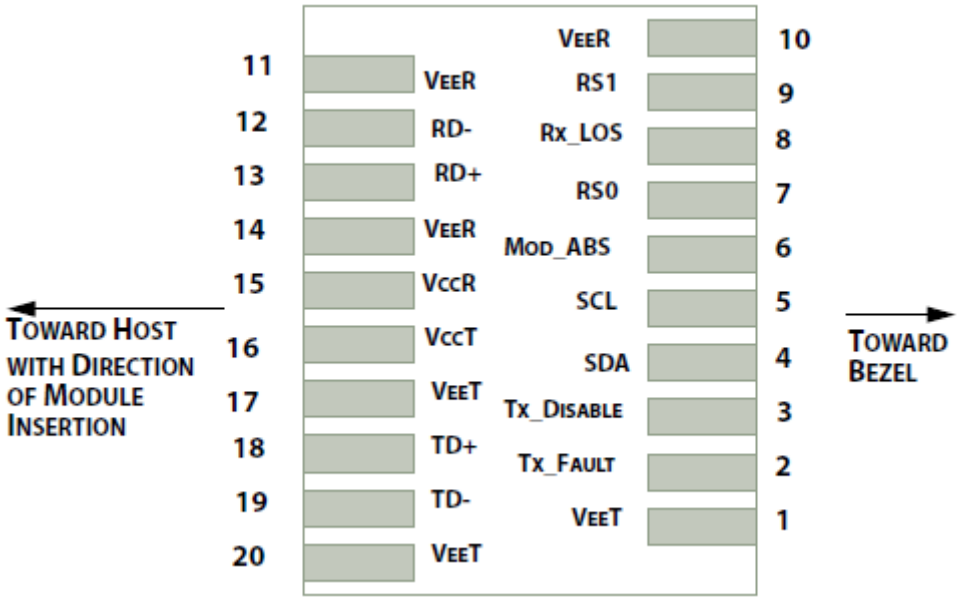
Pin	Logic.	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		Vcc Rx	+3.3V Power Supply Receiver	2
11	LVCMOSI/O	SCL	2-wire serial interface clock	
12	LVCMOSI/O	SDA	2-wire serial interface data	
13		GND	Ground	1

14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		Vcc Tx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Non-Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Inverted Data Output	
37	CML-I	Tx1n	Transmitter Non-Inverted Data Output	
38		GND	Ground	1

Note:

1. GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Vcc Rx Vcc1 and Vcc Tx may be internally connected with- in the QSFP+ Module module in any combination. The connector pins are each rated for a maximum current of 500 mA.

● Host PCB SFP+ pad contact assignment



● SFP+ Module and Host Electrical PinDescriptions

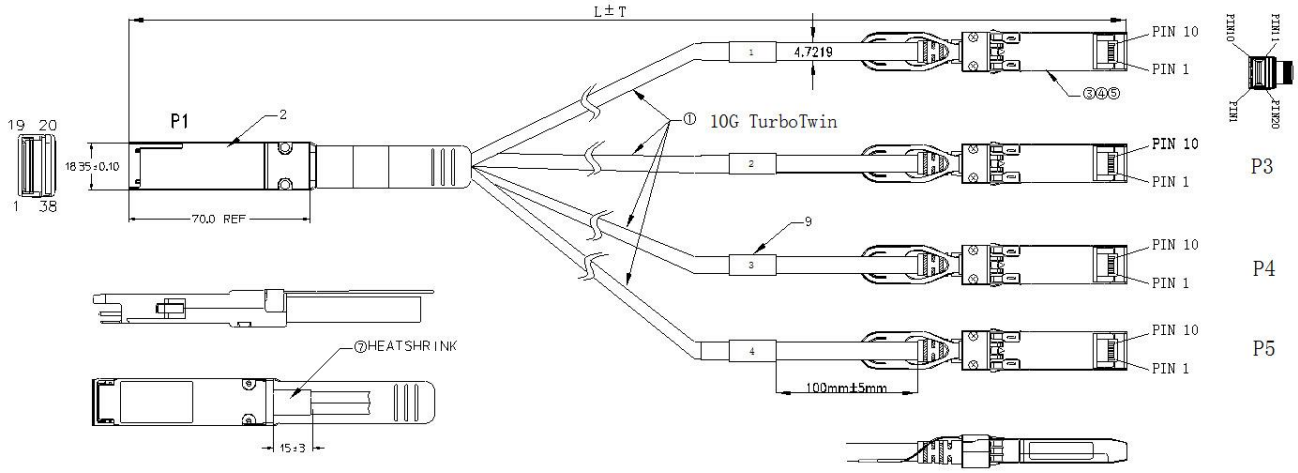
Pin	Logic	Symbol	Name/Description	Note
1		VeeT	Transmitter Ground	
2	LV-TTL-O	TX_Fault	N/A	1
3	LV-TTL-I	TX_DIS	Transmitter Disable	2
4	LV-TTL-I/O	SDA	Tow Wire Serial Data	
5	LV-TTL-I	SCL	Tow Wire Serial Clock	
6		MOD_DEF0	Module present, connect to VeeT	
7	LV-TTL-I	RS0	N/A	1
8	LV-TTL-O	LOS	LOS of Signal	2
9	LV-TTL-I	RS1	N/A	1
10		VeeR	Reciever Ground	
11		VeeR	Reciever Ground	
12	CML-O	RD-	Reciever Data Inverted	
13	CML-O	RD+	Reciever Data Non-Inverted	
14		VeeR	Reciever Ground	
15		VccR	Reciever Supply 3.3V	
16		VccT	Transmitter Supply 3.3V	
17		VeeT	Transmitter Ground	
18	CML-I	TD+	Transmitter Data Non-Inverted	
19	CML_I	TD-	Transmitter Data Inverted	
20		VeeT	Transmitter Ground	

Note

1. Signals not supported in SFP+ Copper pulled-down to VeeT with 30K ohms resistor

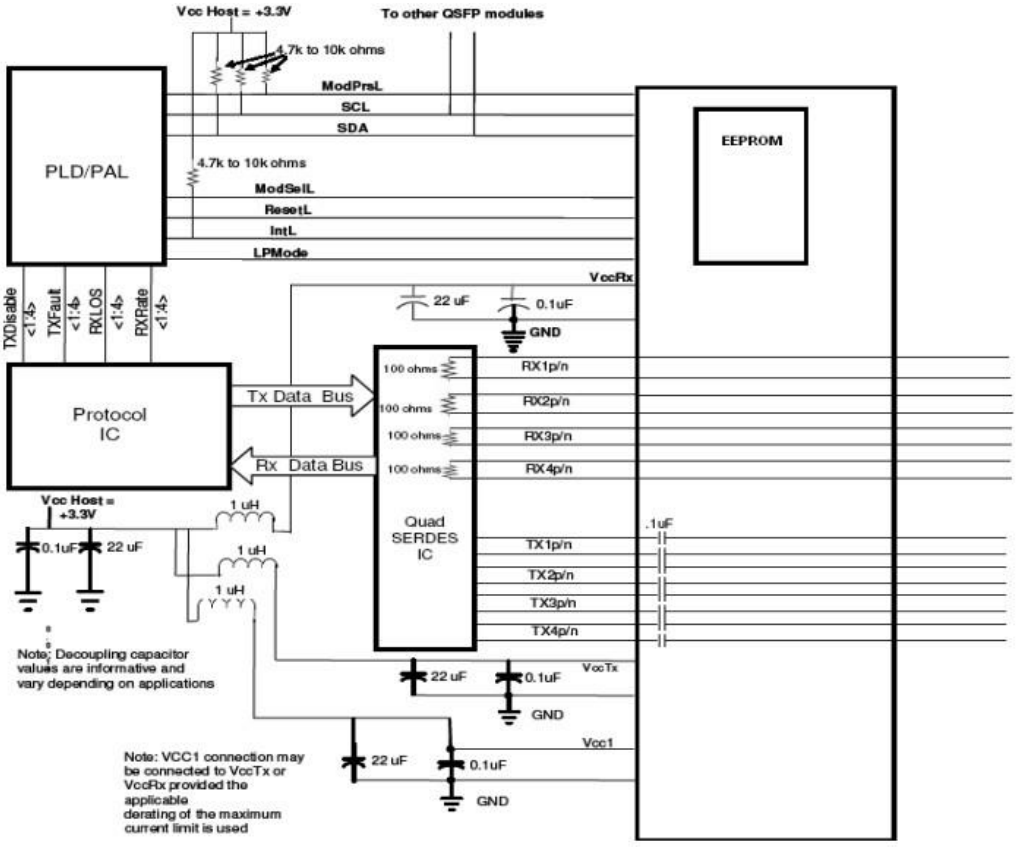
2. Passive cable assemblies do not support LOS and TX_DIS (SFF-8431 2.4)

● Mechanical Dimensions:



Mechanical Drawing

● QSFP+ Host Board Schematic for passive copper cables



FIBERWAN reserves the right to make changes to the products or information contained herein without notice. No liability is assumed as a result of their use or application. No rights under any patent accompany the sale of any such products or information.