

Features:

- ✧ Compliant with QSFP-DD TO 8 QSFP MSA Specification Rev 3.4;
- ✧ SFF-8679 electrical interface compliant;
- ✧ SFF-8636 management interface support;
- ✧ Support 50G (PAM4) electrical data rates/channel;
- ✧ I2C for EEPROM communication; Pull to Release latch design;
- ✧ Excellent EMI/EMC performance 360 degree cable shield termination;
- ✧ Advantage dual side pre-solder automated assembly technologies;
- ✧ Low loss, stronger mechanical features, more flexible;
- ✧ QSFP-DD TO 8 QSFP modules will be

backwards compatible, allowing them to support existing QSFP modules and provide flexibility for end users and system designers;

Applications:

- ✧ Data center & Networking Equipment
- ✧ Servers/Storage Devices
- ✧ High Performance Computing (HPC)
- ✧ Switches/Routers

Standards Compliance

- ✧ IEEE802.3Bj,By,IEEE802.3CD
- ✧ RoHS Compliant

● Ordering information

Part Number	SPEED	Specifications			Categories	DAC or ACC
		Length(mm)	Gauge(awg)	Tolerance (mm)		
FWTD-400G-8-01	400G	1.0	30	+50/-25	QSFP-DD TO 8 QSFP	DAC
FWTD-400G-8-02	400G	2.0	28	+80/-35		DAC
FWTD-400G-8-03	400G	3.0	27	+80/-35		DAC

● Product Description:

In an effort to keep up with the demands of higher performance and increasing amounts of memory bus bandwidth, FIBERWAN designers are working to revise, extend and update the solution. FIBERWAN 400Gbe QSFP-DD TO 8 QSFP passive cable assembly can provide new generation performance of QSFP by higher data transfer rate. At the same time, FIBERWAN QSFP-DD TO 8 QSFP cable choose dual side drain cable and self-designed PCBA, provide low loss, less skew and better NEXT. 360 degree EMI crimping shielding and Zinc Die-cast shell designing make the product high-performance. And all the designing is based on the industry standard specifications, such as SFF-8679, SFF-8636 and QSFP-DD TO 8 QSFP MSA specification rev 4.0.

● Schematic:

WIRING TABLE—QSFP-DD TO 8SFP

CONN-P0		SHIELD BRAIDING	CONN-P1—P8	
SHELL			SHELL	
GND		[Shield Braiding Diagram]	GND(RX)	P1
TX1n P37			P12 RDn	
TX1p P36			P13 RDp	
GND			GND(RX)	
GND			GND(TX)	P2
RX1p P17			P18 TDp	
RX1n P18			P19 TDn	
GND			GND(TX)	
GND			GND(RX)	P3
TX2n P2			P12 RDn	
TX2p P3			P13 RDp	
GND			GND(RX)	
GND			GND(TX)	P4
RX2p P22			P18 TDp	
RX2n P21			P19 TDn	
GND			GND(TX)	
GND		GND(RX)	P5	
TX3n P34		P12 RDn		
TX3p P33		P13 RDp		
GND		GND(RX)		
GND		GND(TX)	P6	
RX3p P14		P18 TDp		
RX3n P15		P19 TDn		
GND		GND(TX)		
GND		GND(RX)	P7	
TX4n P5		P12 RDn		
TX4p P6		P13 RDp		
GND		GND(RX)		
GND		GND(TX)	P8	
RX4p P25		P18 TDp		
RX4n P24		P19 TDn		
GND		GND(TX)		

CONN-P0		SHIELD BRAIDING	CONN-P1—P8	
SHELL			SHELL	
GND		[Shield Braiding Diagram]	GND(RX)	P5
TX5n P75			P12 RDn	
TX5p P74			P13 RDp	
GND			GND(RX)	
GND			GND(TX)	P6
RX5p P55			P18 TDp	
RX5n P56			P19 TDn	
GND			GND(TX)	
GND			GND(RX)	P7
TX6n P40			P12 RDn	
TX6p P41			P13 RDp	
GND			GND(RX)	
GND			GND(TX)	P8
RX6p P60			P18 TDp	
RX6n P59			P19 TDn	
GND			GND(TX)	
GND		GND(RX)	P5	
TX7n P72		P12 RDn		
TX7p P71		P13 RDp		
GND		GND(RX)		
GND		GND(TX)	P6	
RX7p P52		P18 TDp		
RX7n P53		P19 TDn		
GND		GND(TX)		
GND		GND(RX)	P7	
TX8n P43		P12 RDn		
TX8p P44		P13 RDp		
GND		GND(RX)		
GND		GND(TX)	P8	
RX8p P63		P18 TDp		
RX8n P62		P19 TDn		
GND		GND(TX)		

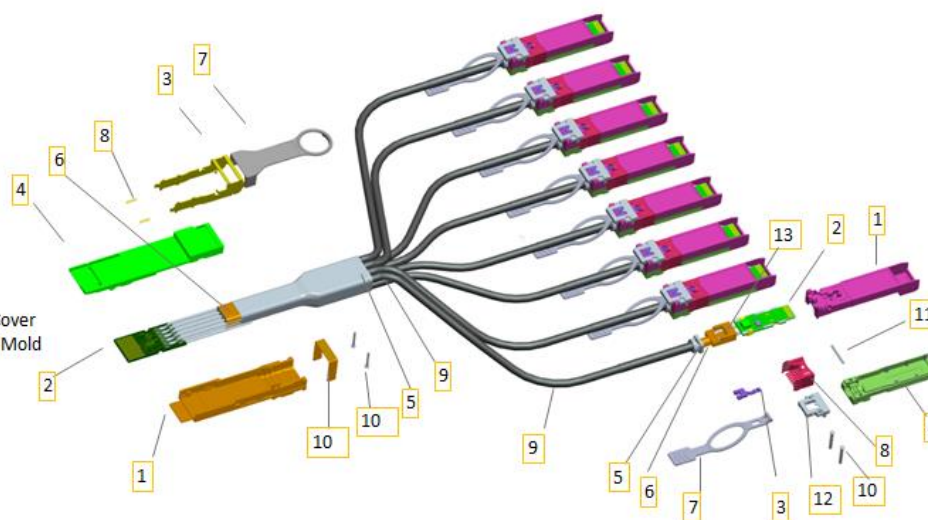
● Cable Assembly Characteristics

QSFP-DD TO 8 QSFP

QSFP-DD TO 8SFP

[Exploded View](#)

- 1.Bot Back Shell
 - 2.PCBA(QDD)
 - 3.SUS304 LATCH
 - 4.Top Back Shell
 - 5.Heat Tube
 - 6.Copper foil
 - 7.Pull LATCH
 - 8.Spring
 - 9.Raw Cable
 - 10.Lock LATCH
 - 11.Rivet
-
- 1.Bot Back Shell
 - 2.PCBA(QSFP28)
 - 3.LATCH
 - 4.TOP Shell
 - 5.SR
 - 6.Copper foil
 - 7.Pull Tap
 - 8.EMI Spring
 - 9.Raw Cable
 - 10. Rivet
 - 11.DOWEL
 - 12.Rear Cover
 - 13.Insert Mold



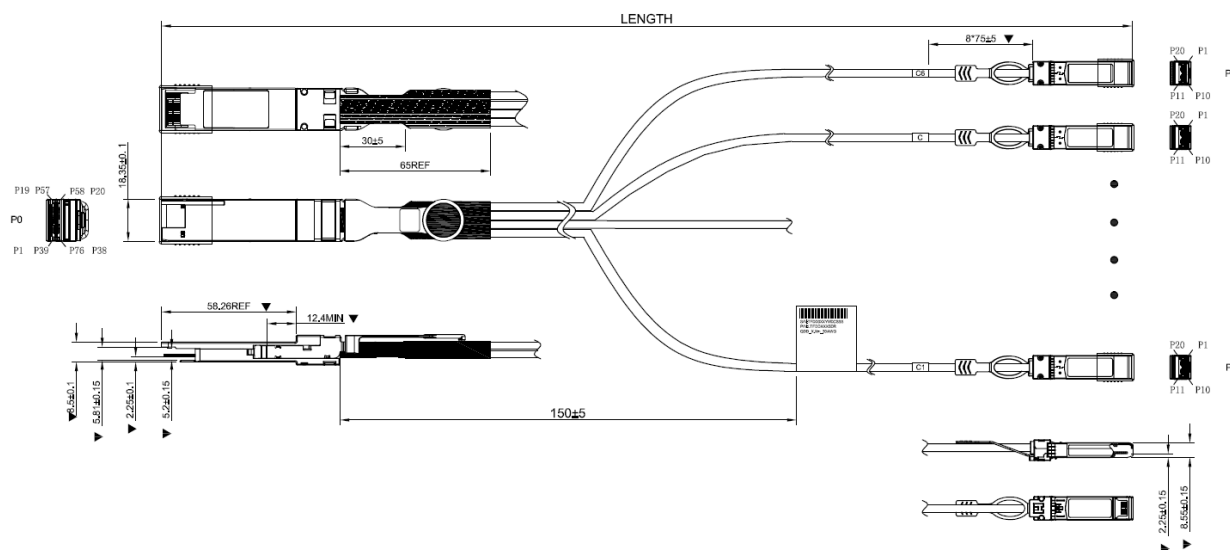
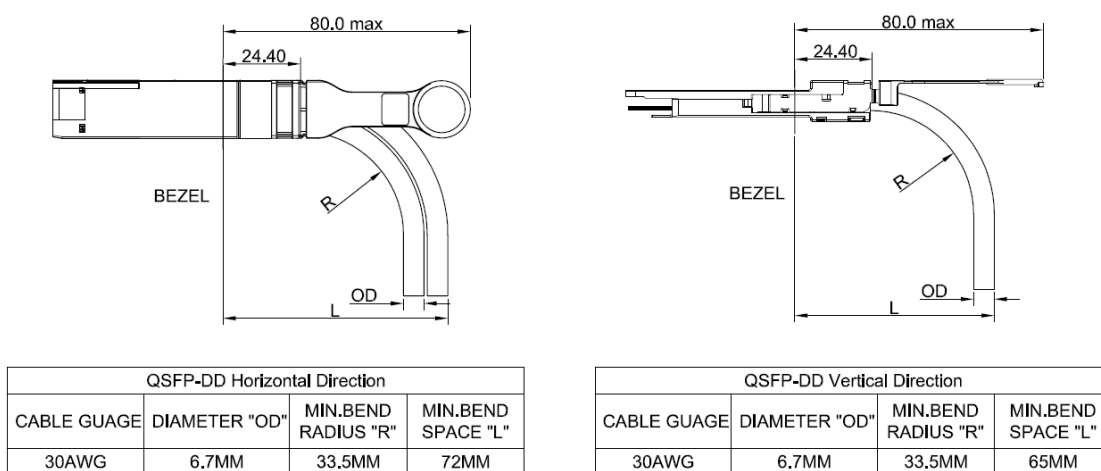


Figure 1 QSFP-DD TO 8 QSFP Mechanical Structure

QSFP-DD 30AWG



QSFP-DD 28AWG

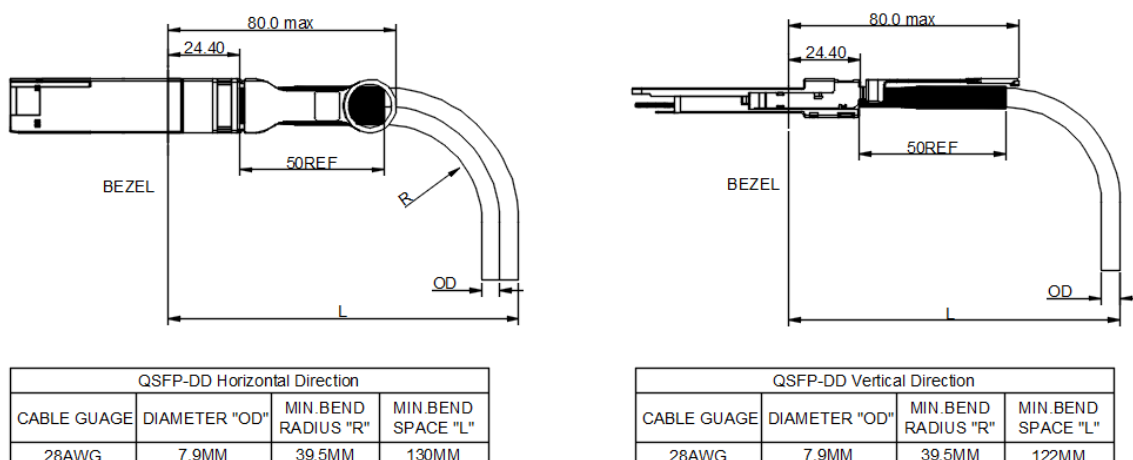


Figure 2 Horizontal and Vertical Bend Radius

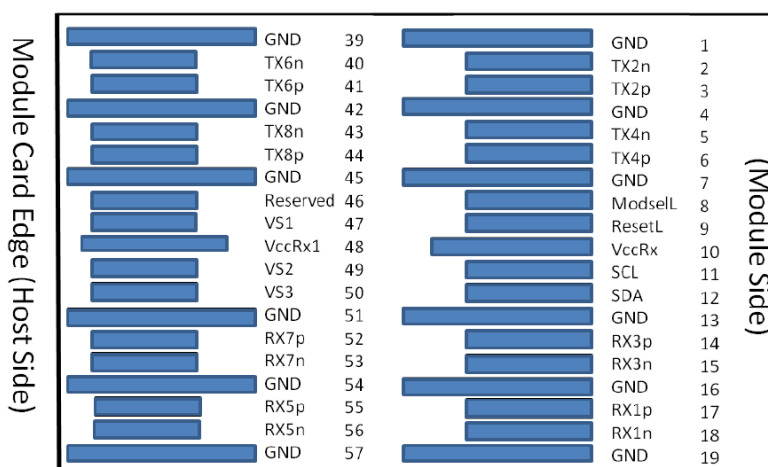
● Mechanical Structure Characteristics Of Plug

- ✧ Raw Cable -- Support 28~30AWG, 100ohm, Silver plated, vw-1, RoHS.
- ✧ PCB –High Speed Very low loss material M6,8 Layers Design; Gold finger plated gold 30u" min., nickel plated 150~700u"; pad: immersion gold 1u" min., nickel plated 100u"min. 94v-0, RoHS2.0;
- ✧ Upper shell -- Zinc Die-cast, with Cu plated 280u" min. overall and Ni plated 120u" min.
- ✧ Bottom shell -- Zinc Die-cast, with Cu plated 280u" min. overall and Ni plated 120u" min.
- ✧ Latch-- Stainless steel ,SUS304 + PA66 CM3004,black;
- ✧ Spring -- Stainless steel ,SUS301EH;
- ✧ Rivet -- Stainless Steel, SUS304;
- ✧ SR (Strain Relief) -- PVC, 45P, BLACK, RoHS.
- ✧ Dust Cover—PVC, 60P, Blue, ANTI-STATIC, RoHS.

● Electrical Design

The electrical design of the QSFP-DD TO 8 QSFP cable assembly is fully compliant to QSFP-DD TO 8 QSFP Hardware Rev4.0 specifications. The electrical design included: a low loss design printed circuit board, DC block capacitances in the Rx channel, and EEprom chips for the management. Pin layout and function definition are shown in Figure 3 and Table 1.

Bottom side viewed from bottom



Top side viewed from top

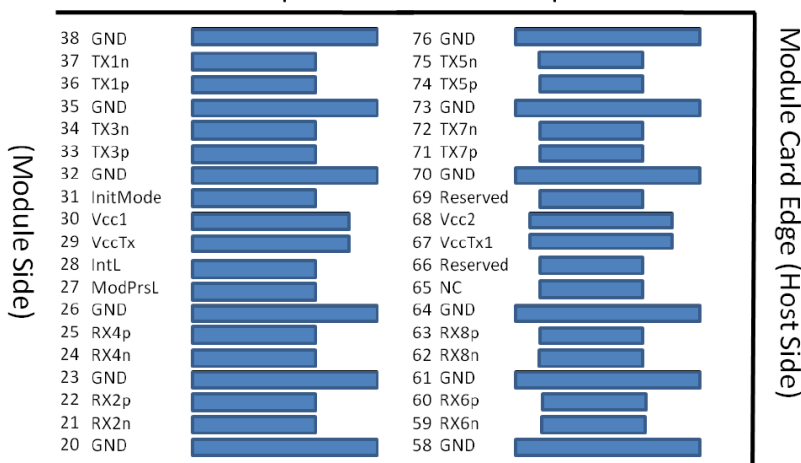


Figure 3 QSFP-DD TO 8 QSFP Pin Define

Table 1 QSFP-DD TO 8 QSFP Pin Function Definition

Pin	Logic	Symbol	Name/Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	
12	LVC MOS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply Transmitter	2
30		Vccl	+3.3V Power Supply	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1

43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	3
47		VSI	Module Vendor Specific 1	3
48		VccRx1	3.3V Power Supply	2
49		VS2	Module Vendor Specific 2	3
50		VS3	Module Vendor Specific 3	3
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69		Reserved	For future use	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

Note 1: QSFP-DD TO 8 QSFP uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD TO 8 QSFP module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD TO 8 QSFP pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

● 2-Wires EEPROM Interface

The QSFP-DD TO 8 QSFP passive cable EEPROM is compliant with CMIS3.0 specification. Each connector contains a 256 bytes EEPROM at device address A0(h). The information for addresses 0 to 255 is listed below, see table 3. This information can be tailored to any customer request. Any address can be altered to display customer specific information.

Table 2 QSFP-DD TO 8 QSFP EEPROM MAP

A0h address	Name	Value	Description
0	Identifier	18	Type of Serial Module -- See SFF-8024,19h:OSFP 8X Pluggable Transceiver
1	Version ID	30	the upper nibble is the whole number part and the lower nibble is the decimal part.Example: 21h indicates version 2.1.
2	Flat_mem	80	Upper memory flat or paged.0b=Paged memory 1b=Flat memory (only page 00h implemented)
	CLEI present		CLEI code present in upper page 00h
	Reserved		Reserved
	TWI Maximum speed		Indicates maximum two-wire serial speed supported by module 00b=Module supports up to 400 KHz 01b=Module supports up to 1 MHz 10b=Reserved 11b=Reserved
	Reserved		Reserved
3	Reserved	03	Reserved
	Module state		Current state of Module 001b:ModuleLowPwr state(Flat memory passive cable assemblies)
	Interrupt		Digital state of IntL Interrupt output signal 0b=IntL asserted 1b=IntL not asserted (default)
4~7	Bank 0 lane flag	00	Indicates that one or more of the flag bits from bank 0
8	Reserved	00	Reserved
	Module state changed flag		Indicates change of Module state
9~13	Module Interrupt Flags	00	Module Interrupt Flags
14~25	Module monitors	00	Module monitors Temperature MSB
26~30	Module Global Controls	00	ForceLowPwr,Software Reset,Custom
31~36	Module Level Flag Masks	00	Module Level Flag Masks
37~63	Reserved	00	Reserved
64~84	Custom	00	Custom
85	Module Type Encodings	03	00h:Undefined 01h:Optical Interfaces: MMF 02h:Optical interfaces: SMF 03h:Passive Cu 04h:Active Cable 005:Base-T
86	Module Host Electrical interface codes(ApSel:0001b)	1D	1A:100GBASE-CR4 NRZ 1D:400G CR8 PAM4
87	Module Media interface codes(ApSel:0001b)	01	01:Copper cable

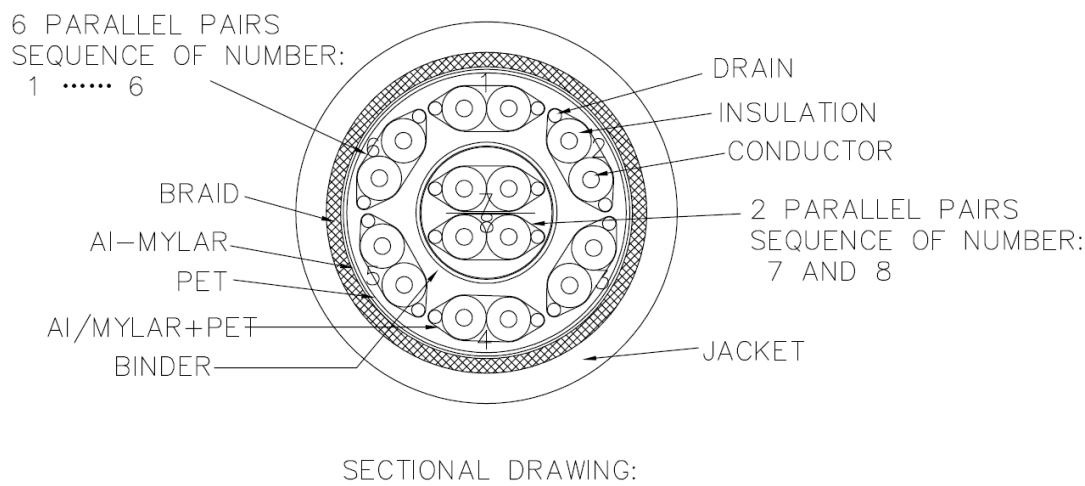
88	Host/Media Lane Count(ApSel:0001b)	88	7-4:Host Lane Count 3-0:Media Lane Count
89	Lane Assignment(ApSel:0001b)	00	code 1:if application is allowed on a given host lane.bits0-7 correspond to host lanes 1-8
90	Module Host Electrical interface codes(ApSel:0010b)	00	Module Host-Media Interface Advertising Codes
91	Module Media interface codes(ApSel:0010b)	00	Module Host-Media Interface Advertising Codes
92	Host/Media Lane Count(ApSel:0010b)	00	Module Host-Media Interface Advertising Codes
93	Lane Assignment(ApSel:0010b)	00	Module Host-Media Interface Advertising Codes
94	Module Host Electrical interface codes(ApSel:0011b)	00	Module Host-Media Interface Advertising Codes
95	Module Media interface codes(ApSel:0011b)	00	Module Host-Media Interface Advertising Codes
96	Host/Media Lane Count(ApSel:0011b)	00	Module Host-Media Interface Advertising Codes
97	Lane Assignment(ApSel:0011b)	00	Module Host-Media Interface Advertising Codes
98	Module Host Electrical interface codes(ApSel:0100b)	00	Module Host-Media Interface Advertising Codes
99	Module Media interface codes(ApSel:0100b)	00	Module Host-Media Interface Advertising Codes
100	Host/Media Lane Count(ApSel:0100b)	00	Module Host-Media Interface Advertising Codes
101	Lane Assignment(ApSel:0100b)	00	Module Host-Media Interface Advertising Codes
102	Module Host Electrical interface codes(ApSel:0101b)	00	Module Host-Media Interface Advertising Codes
103	Module Media interface codes(ApSel:0101b)	00	Module Host-Media Interface Advertising Codes
104	Host/Media Lane Count(ApSel:0101b)	00	Module Host-Media Interface Advertising Codes
105	Lane Assignment(ApSel:0101b)	00	Module Host-Media Interface Advertising Codes
106	Module Host Electrical interface codes(ApSel:0110b)	00	Module Host-Media Interface Advertising Codes
107	Module Media interface codes(ApSel:0110b)	00	Module Host-Media Interface Advertising Codes
108	Host/Media Lane Count(ApSel:0110b)	00	Module Host-Media Interface Advertising Codes
109	Lane Assignment(ApSel:0110b)	00	Module Host-Media Interface Advertising Codes

110	Module Host Electrical interface codes(ApSel:0111b)	00	Module Host-Media Interface Advertising Codes
111	Module Media interface codes(ApSel:0111b)	00	Module Host-Media Interface Advertising Codes
112	Host/Media Lane Count(ApSel:0111b)	00	Module Host-Media Interface Advertising Codes
113	Lane Assignment(ApSel:0111b)	00	Module Host-Media Interface Advertising Codes
114	Module Host Electrical interface codes(ApSel:1000b)	00	Module Host-Media Interface Advertising Codes
115	Module Media interface codes(ApSel:1000b)	00	Module Host-Media Interface Advertising Codes
116	Host/Media Lane Count(ApSel:1000b)	00	Module Host-Media Interface Advertising Codes
117	Lane Assignment(ApSel:1000b)	00	Module Host-Media Interface Advertising Codes
118~125	Password Entry and Change	00	Password Entry and Change
126	Bank Select Byte	00	The module shall ignore the Bank Select byte if the Page Select byte is outside of the 10h to 1Fh range (inclusive).In this case the Bank Select byte shall revert to bank 0 and read/write operations shall be to bank 0.
127	Page Select Byte	00	Writing the value of a non-supported page shall not be accepted by the module. In such cases the Page Select byte shall revert to 0 and read/write operations shall be to upper page 00h.
128	Identifier	18	Identifier Type of Module
129~144	Vendor name	*	Vendor name(ASCII)
145	Vendor OUI	3C	Vendor IEEE company ID
146		18	
147		A0	
148~163	Vendor PN	*	Part number provided by vendor(ASCII)
164	Vendor rev	41	Vendor rev A
165		20	Vendor rev A
166~181	Vendor SN	*	Vendor Serial Number(ASCII)
182~189	Date code	*	Date code(ASCII)
190~199	CLEI code	00	Common Language Equipment Identification code
200	Module Card Power Class	00	000: Power class 1; 001: Power class 2 010: Power class 3; 011: Power class 4 100: Power class 5; 101: Power class 6 110: Power class 7; 111: Power class 8
201	Max Power	06	Maximum power consumption in multiples of 0.25 W rounded up to the next whole multiple of 0.25 W
202	Cable assembly Length Lenth multiplier field	*	Multiplier for value in bits 5-0. 00 = multiplier of .1 01 = multiplier of 1 10 = multiplier of 10 11 = multiplier of 100
	Cable assembly Length Base Length field		Link length base value. To calculate actual link length use multiplier in bits 7-6.

203	Media connector Type	23	Type of connector present in the module. See SFF-8024 for codes. 23h: Non-separable Connector
204	Copper cable Attenuation 5GHz	*	Passive copper cable attenuation at 5 GHz in 1 dB increments
205	Copper cable Attenuation 7GHz	*	Passive copper cable attenuation at 7 GHz in 1 dB increments
206	Copper cable Attenuation 12.89GHz	*	Passive copper cable attenuation at 12.89 GHz in 1 dB increments
207	Copper cable Attenuation 25.8GHz	*	Passive copper cable attenuation at 25.8 GHz in 1 dB increments
208	Reserved	00	Reserved
209	Reserved	00	Reserved
210	Near end implementation lane 8	00	0b= Lane 8 implemented in near end 1b= Lane 8 not implemented in near end
211	Reserved	02	Reserved
	Implemented lanes in far end		See Table 27 for config code of discrete far end connectors
212	Media interface technology	0A	0A: Copper cable unequalized
213~220	Reserved	00	Reserved
221	Custom	00	Custom
222	Checksum	*	Include bytes 128-221
223~251	User custom info NV	00	User custom info NV
252~255	User custom info NV	00	User custom info NV

● Bulk Cable Characteristics

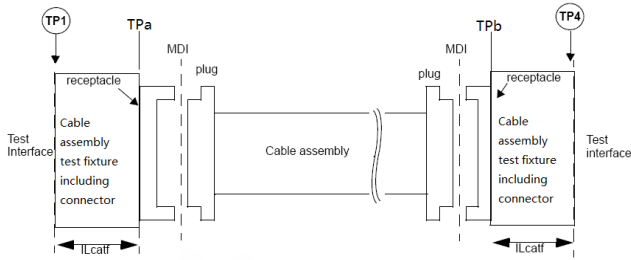
The structure of the cable is shown as the figure, the characteristics of the bulk cable are listed below.



- ✧ Voltage rating: 30V
- ✧ Temperature rating: 80°C;
- ✧ Impedance: Differential mode: 100 +5/-5 ohm @TDR;
- ✧ Delay Skew(INTRA-SKEW): 30ps/5m max;
- ✧ Signal Twin-ax pair cable: Solid Ag plated copper conductor;
- ✧ Braid shielding coverage 85% min.

✧ Jacket material: PVC

● **Qualification Requirement Characteristics**

ITEM		REQUIREMENT	TEST CONDITION
Differential Impedance	Cable Impedance	100 +10/-5 Ω	Rise time of 30ps(at the SMA) (20 % - 80 %).
	Paddle Card Impedance	100 ± 10 Ω	
	Cable Termination Impedance	100 +10 / -15 Ω	
Differential (Input/Output)Return loss SDD11/SDD22		$\text{Return_loss}(f) \geq \left\{ \begin{array}{ll} 16.5-2\sqrt{f} & 0.05 \leq f < 4.1 \\ 10.66-14\log_{10}(f/5.5) & 4.1 \leq f \leq 19 \end{array} \right\}$ <p>Where f is the frequency in GHz Return loss(f) is the return loss at frequency f</p>	10MHz ≤ f ≤ 26.5GHz
Differential to common-mode (Input/Output)Return loss SCD11/SCD22		$\text{Return_loss}(f) \geq \left\{ \begin{array}{ll} 22-(20/25.78)f & 0.01 \leq f < 12.89 \\ 15-(6/25.78)f & 12.89 \leq f \leq 19 \end{array} \right\}$ <p>Where f is the frequency in GHz Return_loss(f) is the Differential to common-mode return loss at frequency f</p>	10MHz ≤ f ≤ 26.5GHz
Common-mode to Common-mode (Input/Output)Return loss SCC11/SCC22		$\text{Return_loss}(f) \geq 2\text{dB} \quad 0.2 \leq f \leq 19$ <p>Where f is the frequency in GHz Return_loss(f) is the common-mode to common-mode return loss at frequency</p>	10MHz ≤ f ≤ 26.5GHz
Differential Insertion Loss		(Differential InsertionLoss Max. For TPa to TPb Including Test fixture)	10MHz ≤ f ≤ 19GHz
		Passive Cable : -17.16dB Min. @13.28GHz	
			10MHz ≤ f ≤ 26.5GHz
Differential to common-mode Conversion Loss-Differential Insertion Loss(SCD21-SDD21)		$\text{Conversion_loss}(f) - \text{IL}(f) \geq \left\{ \begin{array}{ll} 10 & 0.01 \leq f < 12.89 \\ 27-(29/22)f & 12.89 \leq f < 15.7 \\ 6.3 & 15.7 \leq f \leq 19 \end{array} \right\}$ <p>Where f is the frequency in GHz Conversion_loss(f) is the cable assembly differential to</p>	10MHz ≤ f ≤ 26.5GHz

	common-mode conversion loss IL(f) is the cable assembly insertion loss	
ICN	a is the IL@13.28GHz $3 \leq a \leq 7.65$: 9 mV Max $7.65 \leq a \leq 26$: 12.75 - 0.49 *a mV Max	$10\text{MHz} \leq f \leq 26.5\text{GHz}$

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